[[1]](#footnote-1)

CmpE 124 Lab 8: Counter Design with D and JK Flip-Flops

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*Abstract*— Lab eight’s report is a breakdown and analysis of the purpose for lab eight which was to test and analyze the D and JK flip flops. The circuits were built in LogicWorks to learn how the JK and D flip flops functions with different inputs.

# INTRODUCTION

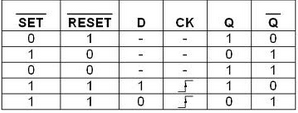
This lab introduced counters using D and JK flip flops. First built a divide by two circuits using D flip flop and the other using a JK flip flops. Secondly a three bit JK Flip Flop ripple down counter was constructed with a count control input. The results were analyzed to fully understand JK and D flip flops.

# Design methodology

## Parts List

* Logic Works
* 74LS74
* 74LS109

## Truth Tables



## Karnaugh Maps

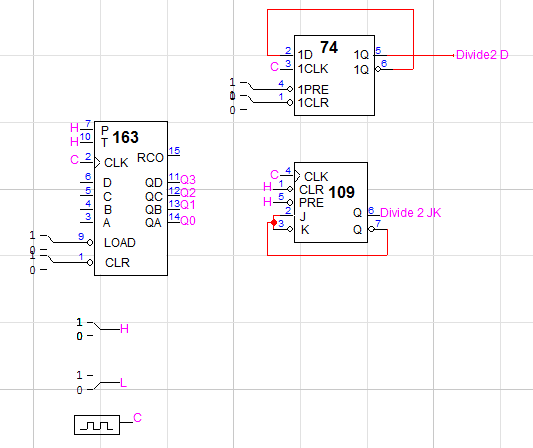
N/A

## Original and Derived Equations

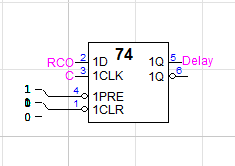
N/A

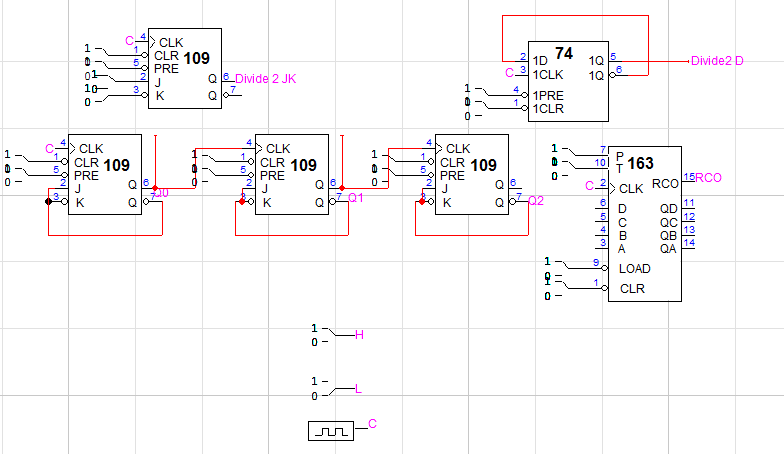
## Schematics

Divide by two circuit using D and JK Flip Flop



One clock period delay circuit for a D flip flop.

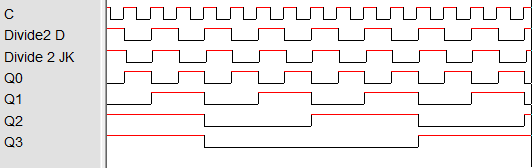


Ripple down counter using a JK flip flop.

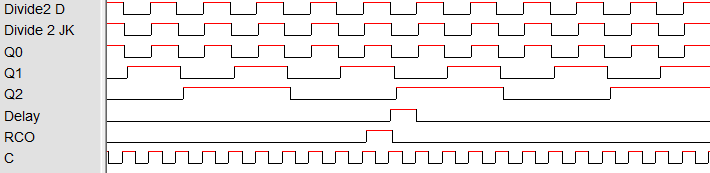
# testing procedures

1. Construct circuits on LogicWorks.
2. Record and Observe outputs.
3. Analyze output on timing waveforms.

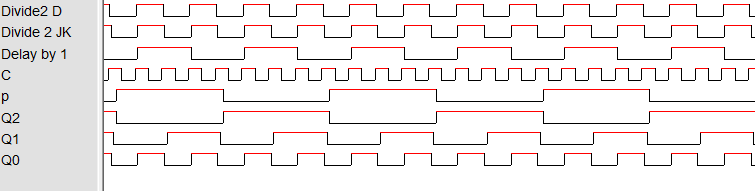
Divide by two circuit for two clock cycle period.



Delay for the divide by two circuit. The delay happens after the RCO reset.



The ripple counter output, the P is an input and will hold the count.



# testing results

The results did match the truth tables which means that the circuit design was correct. The ripple down counter made with the JK flip flop works when the control input P is 1 and when the P is 0 it retains the previous state and continues till p becomes 1. In order to convert the ripple down counter to the ripple up counter we will connect JK input to Q instead, and take out the output across the Q. These flip flops can be used as binary counters and registers.

# Conclusion

LogicWorks helped understand the circuits and how it can be an essential to basic logic design. The quick testing of inputs for potential outputs makes this very efficient way of learning the functions and uses of the D and JK flip flops. The However conducting this experiment with real parts will not result in the same results as not all parts perform at ideal performance.

# appendices and references

N/A

1. Anahit Sarao, indianvip60@gmail.com [↑](#footnote-ref-1)